IN THE CLAIMS:

The following is a complete listing of the claims in this application, reflects all changes currently being made to the claims, and replaces all earlier versions and all earlier listings of the claims:

Claims 1.-11. (Cancelled).

12. (Currently Amended): A method of driving a memory which has a plurality of variable resistors arrayed in a matrix, a plurality of switches connected to the plurality of variable resistors, and a plurality of bit lines arranged on respective rows of the matrix, one terminal of each variable resistor being connected to a corresponding bit line, and the other terminal being connected to a corresponding switch, comprising:

reading information of the bit lines; and

while reading information from a plurality of variable resistors connected to a selected one of the bit lines, selectively keeping one of the plurality of variable resistors connected to the selected bit line.

13. (Previously Presented): A method according to Claim 12, further comprising the step of simultaneously with turning off one of the switches, turning on the switch corresponding to the variable resistor to be read next.